YU-NENG WANG

3rd Year Ph.D. Student in the Electrical Engineering Department at Stanford University
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RESEARCH INTEREST

Hardware/Algorithm Co-design and Design Space Exploration for Unconventional Analog Circuits

EDUCATION

Stanford University CA, USA
Ph.D. student in Electrical Engineering *09/2021 - present*

National Taiwan University (NTU) Taipei, Taiwan
B.S. in Electrical Engineering *09/2016 - 01/2021*

- Cumulative GPA: **4.25**/4.30. (**3rd**/189)

HONORS AND AWARDS

2023 **Government Scholarship to Study Abroad**, Taiwan Ministry of Education.
2021 **Stanford Graduate Fellowship**.
2020 **1st Place**, 2020 CAD Contest at ICCAD.
2020 **Honorable Mention**, ISPD 2020 Contest.
2017-2020 **Dean's List Award, 6 times**, National Taiwan University (offered to **top 5%** students).
2019 **2nd Place**, 2019 CAD Contest at ICCAD.
2019 **College Student Research Scholarship**, Taiwan Minstery of Science and Technology
2019 **Honorable Mention**, 2019 AI CUP, Taiwan Ministry of Education.

SELECTED PUBLICATIONS

1. **Wang, Y.N.**, Glenn Cowan, Ulrich Rührmair, and Sara Achour, 2024. Design of Novel Analog Compute Paradigms with Ark. In 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2 (ASPLOS '24) [paper]
2. **Wang, Y.N.**, Luo, Y.R., Chien, P.C., Wang, P.L., Wang, H.R., Lin, W.H., Jiang, J.H.R. and Huang, C.Y.R., 2021, November. Compatible Equivalence Checking of X-Valued Circuits. In 2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD) (pp. 1-9). IEEE. [paper]

RESEARCH EXPERIENCE

Nonconventional Computing System Laboratory, Prof. Sara Achour CA, USA
Software Techniques for Analog Hardware/Algorithm Co-Design *12/2021-present*

- Devised and implemented Ark, a programming language for the design of novel analog computing paradigms.
- **Enabled progressive incorporation of analog behaviors into computations** and deployed a validator and dynamical system compiler for verifying and simulating computations.
- Codified the design space for a transmission-line-based physical unclonable function, a cellular nonlinear network edge detector, and a oscillator-based computing max-cut solver and **evaluated the impact of nonidealities to the computation in an early design stage**.

Electronic Design Automation Laboratory, Prof. Yao-Wen Chang Taipei, Taiwan
Wafer-Scale Deep Learning Accelerator Placement *12/2019-06/2020*

- Proposed and implemented **an automated mapping and floorplanning algorithm** for a deep learning accelerator.
- Minimized costs of timing, wirelength, and design constraints and won an Honorable Mention in the 2020 ISPD Contest.

System-Level FPGA Routing *02/2019-10/2019*

- Proposed and implemented **a multithreading TDM-ratio-aware routing algorithm and a linear time ratio assigning algorithm** for an FPGA emulation system.
- Provided minimized maximum TDM-ratio solutions efficiently and won the 2^{nd} Place in the 2019 ICCAD Contest.

System-on-a-Chip Verification, Prof. Chung-Yang (Ric) Huang Taipei, Taiwan
X-value Equivalence Checking *03/2020-08/2020*

- Designed and implemented **a compatible equivalence checker** for circuits with X-value.
- Outperformed industrial tools by solving 10 more cases (in 30 test cases) and won the 1^{st} Place in the 2020 ICCAD Contest.

WORK EXPERIENCE

Cadence Design Systems Hsinchu, Taiwan
R&D Intern, Formal Verification Team *07/2020-09/2020*

- Proposed and implemented **a test case generating algorithm and an ECO algorithm** to improve Cadence's products.
- Reduced the ECO patch size by averagely 89% compared to the original algorithm in 10000+ generated test cases.

Microsoft Taipei, Taiwan
R&D Intern, AIoT Team *07/2019-06/2020*

- Integrated **deep learning methods and Azure to provide AI and IoT solutions** for partners of Microsoft.
- Designed and implemented a deep learning model to predict and control the number of sales in convenient stores.
- Devised and implemented a multifaceted computer-aided questionnaire platform for COVID-19 outbreak investigation.

RELATED PROJECTS

Formal Methods for Computer Systems CA, USA
Run S^2QED on PicoRV32 *10/2021-12/2021*

- Performed **bounded model checking on an open-source processor PicoRV32** with Symbolic Quick Error Detection using Symbolic Initial State (S^2QED).
- Verified the core is bug-free within the bound and can catch injected hardware trojan in 11 seconds.

Machine Learning Taipei, Taiwan
News Stance Retrieval System *02/201-09/2019*

- Devised and implemented **a vector space model with Rocchio feedback** to retrieve news based on stance of queries.
- Achieved high Mean Average Precision in public and private sets and won an Honorable Mention in the 2019 AI CUP.

RELEVANT COURSEWORKS

Design Automation Software Techniques for Emerging Hardware Platforms, Physical Design for Nanometer ICs
Analog Circuits Fundamentals of Analog Integrated Circuit (EE 214A), Advanced Integrated Circuit Design (EE 214B).
Digital Circuits Integrated Circuit Design, Integrated Circuits Design Laboratory
Formal Verification Formal Methods for Computer Systems (CS 357S), SoC Verification

SKILLS

Natural Languages Mandarin (Native), English (Proficient, TOEFL score: 110/120).
Programming Languages/Tools C/C++, Python , Verilog, LaTeX.
EDA Tools HSpice, Spectre, nWave, ncverilog, Design Compiler, Conformal LEC, Innovus.